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2SK1750, 1750-Z/2SK1751, 1751-Z

SWITCHING  
N-CHANNEL POWER MOS FET  
INDUSTRIAL USE

DESCRIPTION

The 2SK1750/2SK1751 is N-channel MOS Field Effect Transistor designed for high voltage switching applications.

FEATURES

- Low On-state Resistance  
 $R_{DS(on)} \leq 1.4/1.5 \Omega$  ( $V_{GS} = 10 V, I_D = 2.5 A$ )
- Low  $C_{iss}$   $C_{iss} = 610 pF$  TYP.
- Built-in G-S Gate Protection Diode
- High Avalanche Capability Ratings

QUALITY GRADE

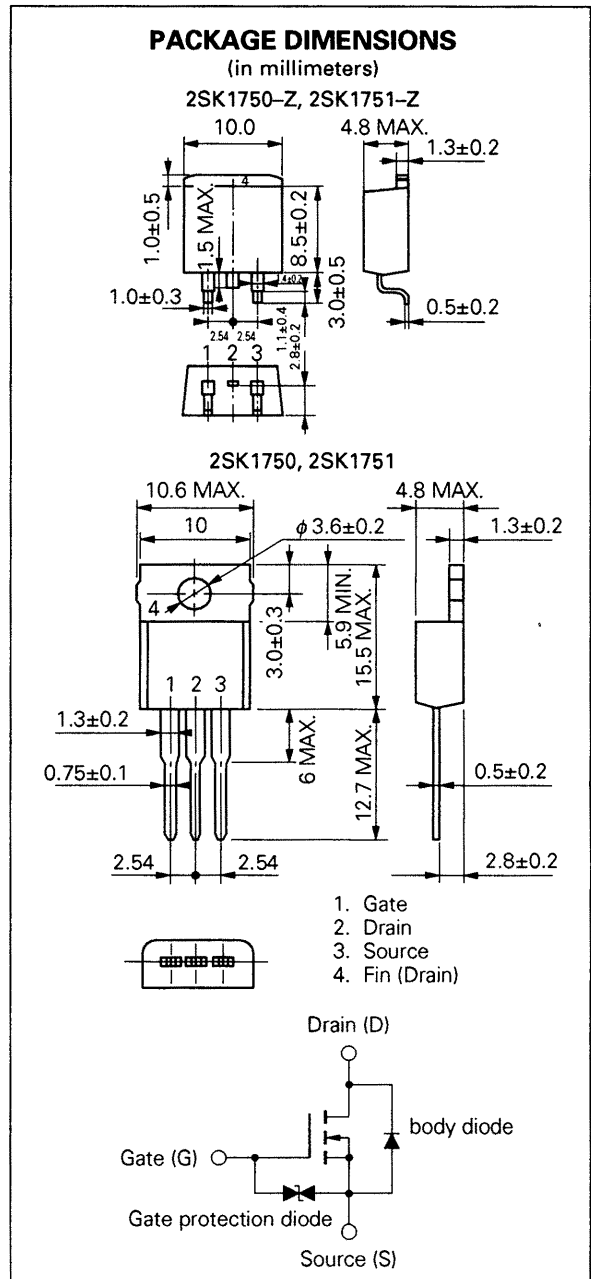
Standard  
Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

ABSOLUTE MAXIMUM RATINGS ( $T_a = 25^\circ C$ )

Drain to Source Voltage	$V_{DSS}$	450/500	V
Gate to Source Voltage	$V_{GSS}$	$\pm 30$	V
Drain Current (DC)	$I_{D(DC)}$	$\pm 5.0$	A
Drain Current (pulse)	$I_{D(pulse)}^*$	$\pm 20$	A
Total Power Dissipation ( $T_c = 25^\circ C$ )	$P_T$	50	W
Channel Temperature	$T_{ch}$	150	$^\circ C$
Storage Temperature	$T_{stg}$	-55 to +150	$^\circ C$
Single Avalanche Current	$I_{AS}^{**}$	7.5	A
Single Avalanche Energy	$E_{AS}^{**}$	40.2	mJ

\*  $PW \leq 10 \mu s$ , Duty Cycle  $\leq 1\%$

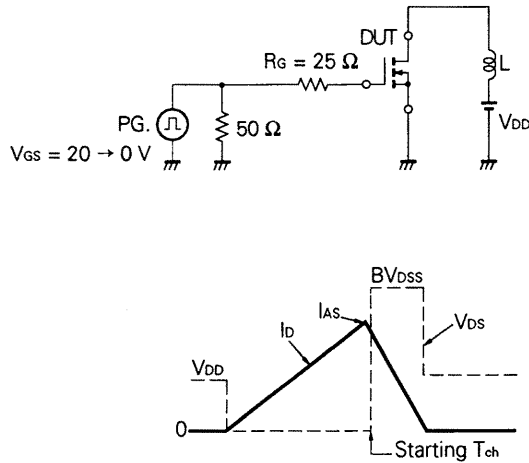
\*\* Starting  $T_{ch} = 25^\circ C$ ,  $R_G = 25 \Omega$ ,  $V_{GS} = 20 V \rightarrow 0$



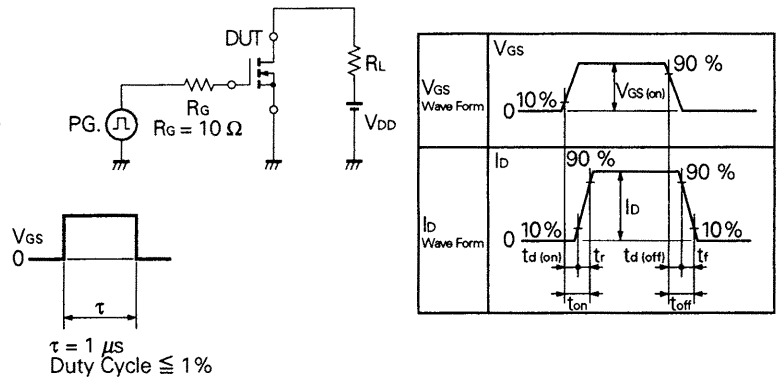
**ELECTRICAL CHARACTERISTICS (T<sub>a</sub> = 25 °C)**

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance (2SK1750)	R <sub>DS(on)</sub>		1.1	1.4	Ω	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 2.5 A
Drain to Source On-state Resistance (2SK1751)	R <sub>DS(on)</sub>		1.2	1.5	Ω	
Gate to Source Cutoff Voltage	V <sub>GS(off)</sub>	2.5		3.5	V	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA
Forward Transfer Admittance	y <sub>fs</sub>	1.0	2.6		S	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 2.5 A
Drain Leakage Current (2SK1750/1751)	I <sub>DSS</sub>			100	μA	V <sub>DS</sub> = 450/500 V, V <sub>GS</sub> = 0
Gate to Source Leakage Current	I <sub>GSS</sub>			±10	μA	V <sub>GS</sub> = ±30 V, V <sub>DS</sub> = 0
Input Capacitance	C <sub>iss</sub>		610		pF	V <sub>DS</sub> = 10 V V <sub>GS</sub> = 0 f = 1 MHz
Output Capacitance	C <sub>oss</sub>		200		pF	
Reverse Transfer Capacitance	C <sub>res</sub>		80		pF	
Turn-On Delay Time	t <sub>d(on)</sub>		15		ns	V <sub>GS</sub> = 10 V V <sub>DD</sub> = 150 V I <sub>D</sub> = 2.5 A, R <sub>G</sub> = 10 Ω R <sub>L</sub> = 60 Ω
Rise Time	t <sub>r</sub>		25		ns	
Turn-Off Delay Time	t <sub>d(off)</sub>		50		ns	
Fall Time	t <sub>f</sub>		20		ns	
Total Gate Charge	Q <sub>G</sub>		22		nC	V <sub>GS</sub> = 10 V I <sub>D</sub> = 5.0 A V <sub>DD</sub> = 400 V
Gate to Source Charge	Q <sub>GS</sub>		5		nC	
Gate to Drain Charge	Q <sub>GD</sub>		13		nC	
Diode Forward Voltage	V <sub>F(S-D)</sub>		0.9		V	I <sub>D</sub> = 5.0 A, V <sub>GS</sub> = 0
Reverse Recovery Time	t <sub>rr</sub>		350		ns	I <sub>D</sub> = 5.0 A, V <sub>GS</sub> = 0
Reverse Recovery Charge	Q <sub>rr</sub>		3.0		μC	di/dt = 50 A/μs

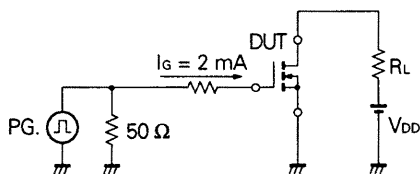
**Test Circuit 1: Avalanche Capability**



**Test Circuit 2: Switching Time**

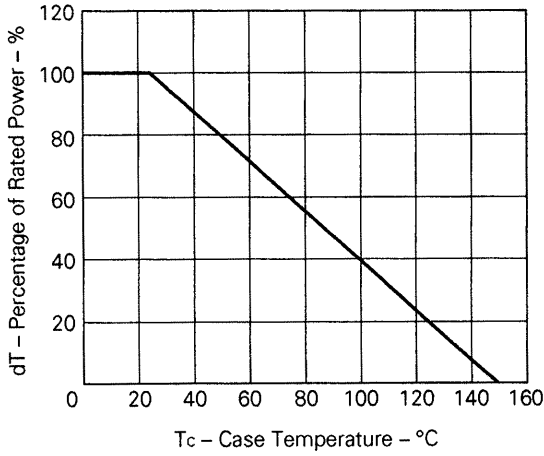


**Test Circuit 3: Gate Charge**

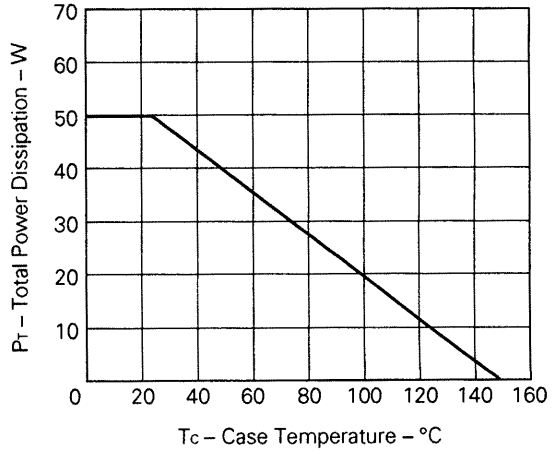


TYPICAL CHARACTERISTICS ( $T_a = 25^\circ\text{C}$ )

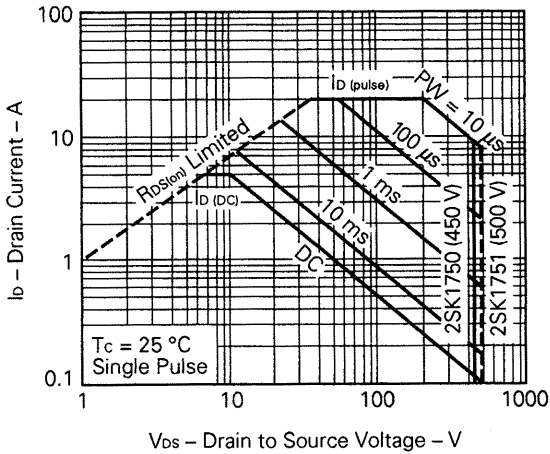
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



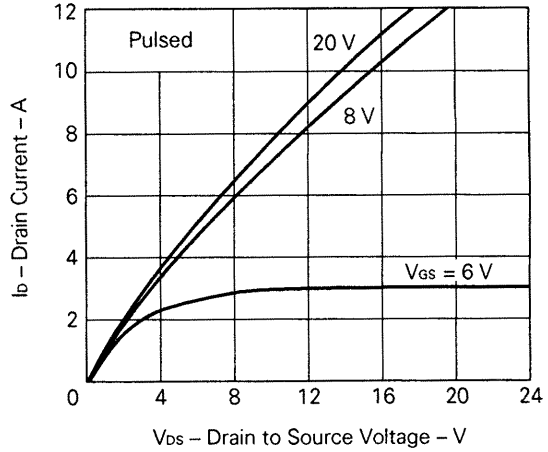
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



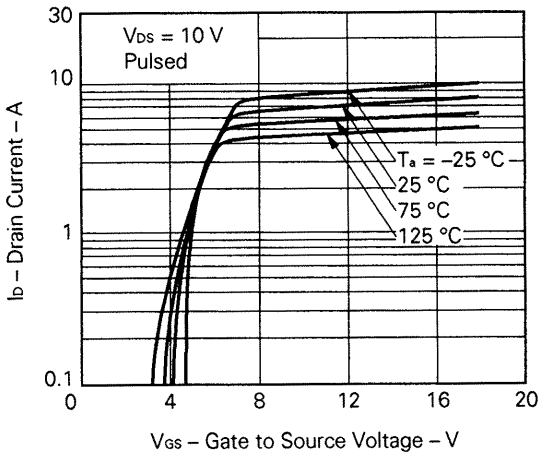
FORWARD BIAS SAFE OPERATING AREA

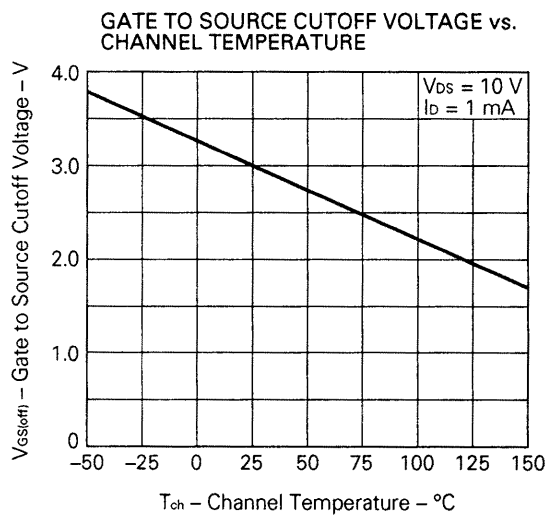
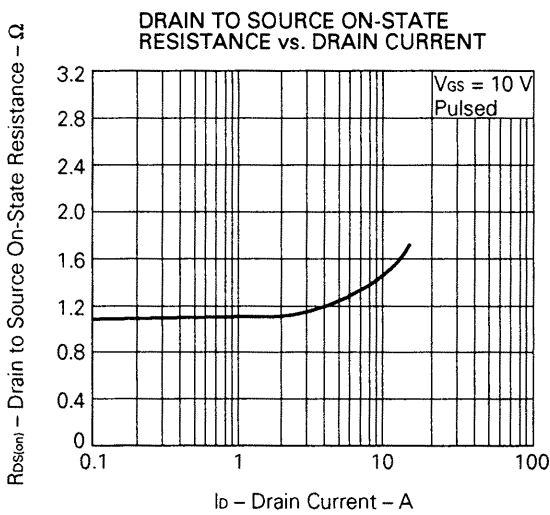
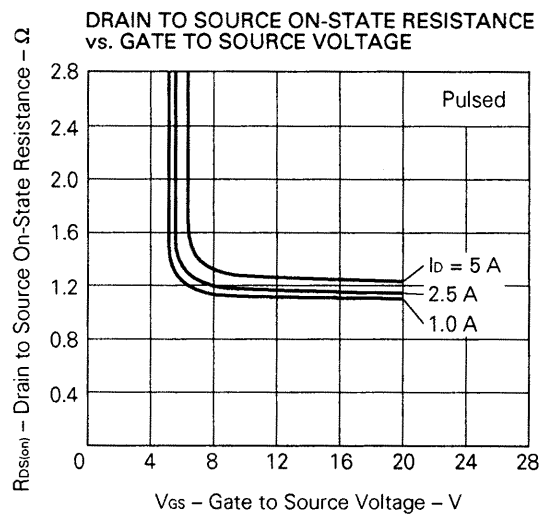
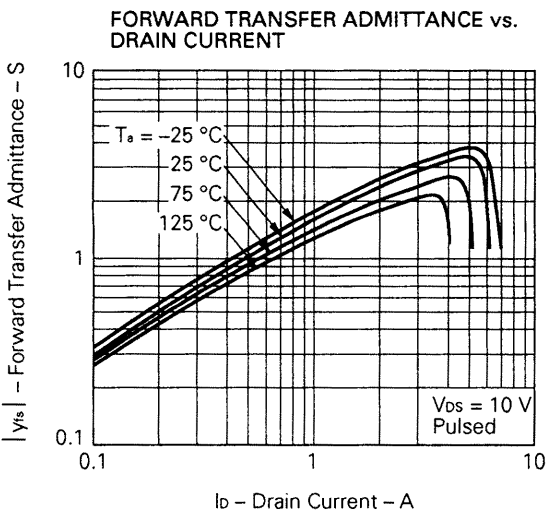
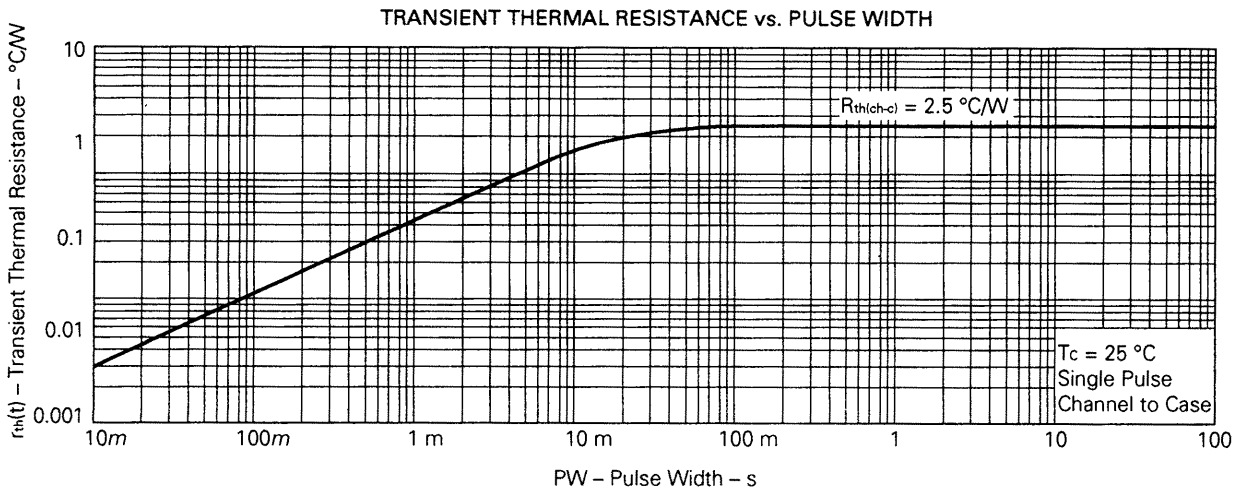


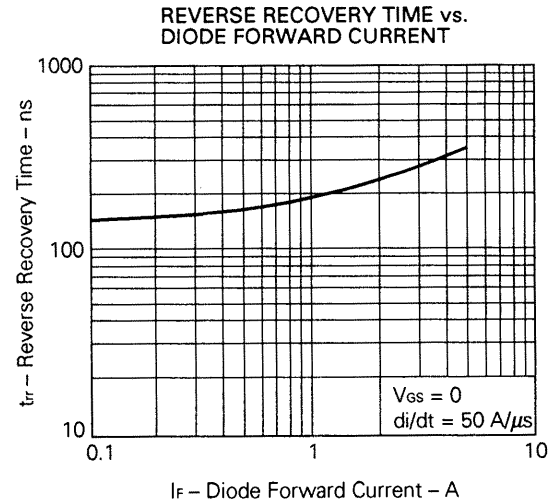
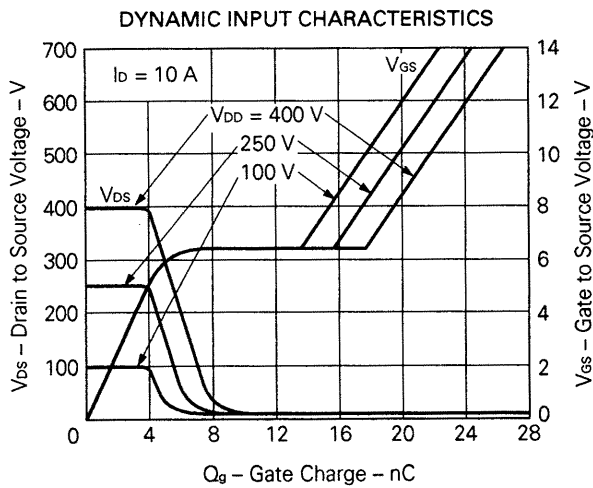
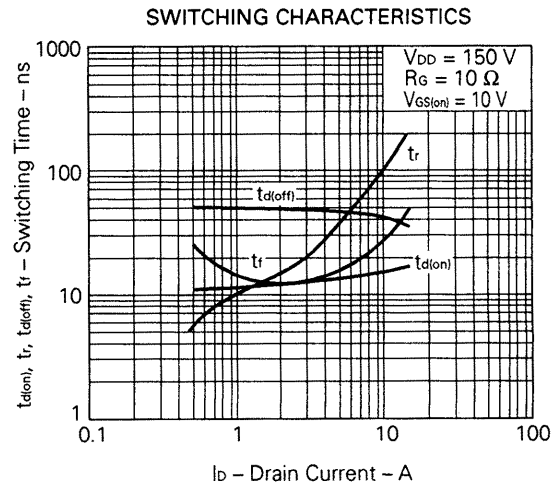
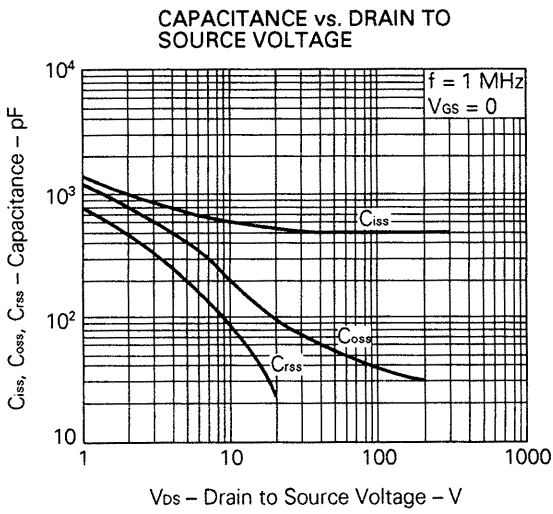
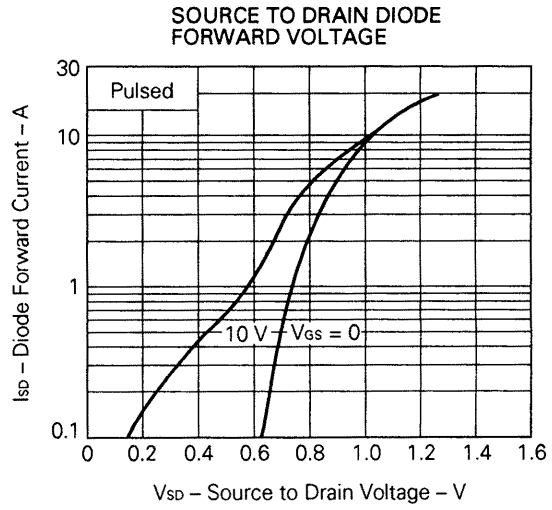
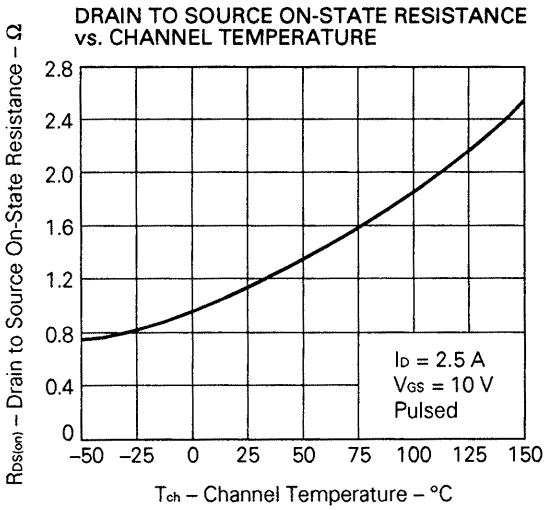
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE

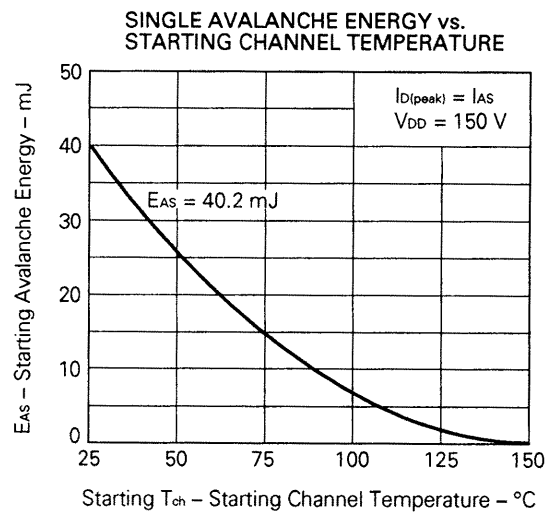
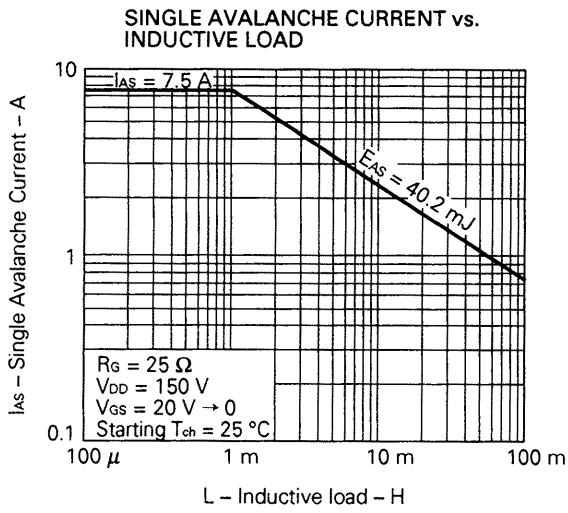


TRANSFER CHARACTERISTICS









**Reference**

Application note name	No.
Safe operating area of Power MOS FET.	TEA-1034
Application circuit using Power MOS FET.	TEA-1035
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207



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